REMARKS

This is a Response to the Office Action mailed August 4, 2008, in which a three (3) month Shortened Statutory Period for Response has been set, due to expire November 4, 2008. Claim 3 has been previously canceled. Claim 13 is currently amended. New claim 21 has been added. No new matter has been added to the application. No fee for additional claims is believed due by way of this Amendment. The Director is authorized to charge any additional fees due by way of this Amendment only, or credit any overpayment, to our Deposit Account No. 19-1090. Upon entry of the amendments herewith, claims 1-2, and 4-21 remain pending.

I. Correction of Typographical Error

Claim 13 has been amended to correct a minor typographical error. A second recitation of "and a data output connected to the initiator interface" has been deleted.

II. Rejections under 35 U.S.C. § 103

At sections 2 through 11 of the Office Action (pages 2-5), claims 1-2, 4-7, and 13-14 were rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over ***O'Connell et al.***, **(U.S. Pat. 6,036,340)**, hereinafter *O'Connell*, in view of ***Fritz et al.***, **(U.S. Pat. Pub. 2002/0016850)**, hereinafter *Fritz*. At sections 12 through 16 and sections 19 through 25 of the Office Action (pages 5-6 and pages 7-9), claims 8-11 were rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over *O'Connell* in view of *Fritz* in further view of ***Sadowski***, **(U.S. Pat. Pub. 2005/0007165)**, hereinafter *Sadowski*. At sections 17 through 18 of the Office Action (pages 6-7), claim 12 was rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over *O'Connell* in view of *Fritz* in further view of ***Cavanna et al.***, **(U.S. Pat. 6,208,703)**, hereinafter *Cavanna*.

Respectful disagreement is made with the above rejections. It is believed that the present independent claims are clearly patentable and that all dependent claims are also patentable.

a. Independent Claim 1

Independent claim 1 is allowable for at least the reason that the cited references do not disclose, teach, or suggest the comparators of claim 1 or the coupling of the comparators to the pointer registers. For example, claim 1 recites, *inter alia*, a "first comparator" that compares values from a write pointer register and a first retiming circuit. Claim 1 also recites, *inter alia*, a "second comparator" that compares values from a read pointer register and a second retiming circuit. The output of the first comparator is used "to increment the count held in the write pointer register." The output of the second comparator is used "to increment the count held in the read pointer register." The *O'Connell* reference has no such comparators and no such mechanism to increment pointers. In fact, the structure taught in *O'Connell* is fundamentally different from the limitations of claim 1. See *O'Connell's* Figure 1. Instead of incrementing his write pointer register 40 based on the current position of the write pointer register 40 and a retiming signal from the read domain, O'Connell increments his write pointer register 40 based a request from an application. See Col. 3, lines 44-49 and Col. 4, lines 17-21. The request from the application is clocked according to *O'Connell's* Application clock (write) domain and not from his PCI clock (read) domain. In this configuration, it is incumbent upon *O'Connell's* application to control the write pointer value to prevent overwriting the Register File 10. See Col. 4, lines 38-58, especially lines 48-53.

Similarly, on the read side, *O'Connell's* read pointer and write pointer are compared according to a PCI clock domain. A difference between the read and write pointer values indicates to an attached PCI machine that data can be read from Register File 10. In response, the attached PCI machine increments the read pointer register by asserting the *mas_start_dma_pci* signal on line 26. See Figure 1; see also Col. 5, line 50 to Col. 6, line 16, especially Col. 6, lines 6-10. Accordingly, it is clear that *O'Connell's* pointer registers are controlled by circuits outside of his Figure 1 interface circuit. This is quite simply different than the elements recited in claim 1.

It is further apparent in *O'Connell* that there are no modifications that could be made to *O'Connell* to render the limitations of claim 1. *O'Connell* sets out to provide an interface that produces handshake signals for circuits outside his interface. The circuits outside

of the application interface are governed by his Application clock domain, and the circuits outside of the PCI interface are governed by his PCI clock domain. See Col. 2, lines 56-62. The handshake circuits of *O'Connell* operate in such a way as to permit the circuits from the Application clock domain to continuously write data without having to wait for the circuits of the PCI clock domain to complete the transaction. In contrast, claim 1 uses circuitry within the interface to control the flow of data through the interface. In claim 1, the write pointer register is incremented only at the synchronizing speed of the first retiming circuit, and the read pointer register is incremented only at the synchronizing speed of the second retiming circuit. External circuits do not increment the pointers of claim 1. In view of the fact that claim 1 recites first and second comparator circuitry having outputs used to increment a write pointer register and a read pointer register respectively and in view of the fact that the cited reference does not disclose, suggest, or teach such circuitry, claim 1 is not allowable over the cited reference. Respectful withdrawal of the rejection is requested.

The *Fritz* reference does nothing to cure the deficiency of *O'Connell*. *Fritz* relates to solving a different problem than *O'Connell*. The bridge circuitry of *O'Connell* matches communication between multiple domains operating at different clock frequencies. In contrast, the circuitry of *Fritz* prevents buffer underrun during communication between multiple domains. *Fritz* addresses the underrun problem by writing data into a buffer, waiting for a "predetermined amount of time," beginning to read data from the buffer, measuring the difference in time from when the write completes and when the read completes, and adjusting the "predetermined amount of time." *See* Abstract.

Fritz's circuitry to solve the underrun problem is shown in Figure 3. A single buffer 310 is used to store communicated data, but no pointers or comparison circuitry is shown. The background section of *Fritz's* specification describes read and write pointers at Paragraph [0005], however, there is no disclosure, suggestion, or teaching of comparators, clock rates, retiming circuits, or pointer increments. Accordingly, the circuits of *Fritz* do not teach the "first comparator" that compares values from a write pointer register and a first retiming circuit, the "second comparator" that compares values from a read pointer register and a second retiming circuit, the output of the first comparator used "to increment the count held in the write pointer

register," and the output of the second comparator used "to increment the count held in the read pointer register."

The addition of *Fritz* does nothing to cure the deficiencies of *O'Connell*. Even if a device that combined the teachings of *O'Connell* with *Fritz* were created, the device would still not have circuitry including a "first comparator" that compares values from a write pointer register and a first retiming circuit, a "second comparator" that compares values from a read pointer register and a second retiming circuit, and the output of the first comparator being used "to increment the count held in the write pointer register," and the output of the second comparator being used "to increment the count held in the read pointer register." For at least these reasons, *O'Connell* and *Fritz* combined do not teach the elements recited in claim 1, and therefore, independent claim 1 is in condition for allowance.

b. Dependent Claim 13

Dependent claim 13, as amended, recites, *inter alia*, a bridge circuit "further comprising a second storage buffer circuit having a data input connected to the target interface and a data output connected to the initiator interface." The cited *Fritz* reference contains no such limitation. More particularly, *Fritz* shows only a single buffer 310 in Figure 3 along with supporting structure such as a physical layer adapter 300, a synchronization unit 312, an underrun prevention unit 324, and a control unit 322. Accordingly, for at least the reason that *Fritz* does not disclose, teach, or suggest a second storage buffer circuit, claim 13 is allowable over the cited reference.

c. Independent Claim 15

It is further apparent that even though the language of claim 15 is not identical to that of claim 1, the nonobviousness of claim 15 will be apparent in view of the above remarks. More specifically, independent claim 15 recites, *inter alia*, a "first comparator" that compares values from a write pointer register and a first retiming circuit. Claim 15 also recites, *inter alia*, a "second comparator" that compares values from a read pointer register and a second retiming circuit. The output of the first comparator is used "to increment the count held in the write

pointer register." The output of the second comparator is used "to increment the count held in the read pointer register." As discussed herein, the cited references do not disclose, teach, or suggest these features. Accordingly, claim 15 is in condition for allowance.

III. New Claim 21

New independent claim 21 is allowable for at least the reason that the cited references do not have a "first comparator" that compares values from a write pointer register and a first retiming circuit and a "second comparator" that compares values from a read pointer register and a second retiming circuit, wherein the output of the first comparator is used "to increment the count held in the write pointer register," and the output of the second comparator is used "to increment the count held in the read pointer register." As discussed herein, the cited references do not disclose, teach, or suggest these features. Accordingly, claim 21 is in condition for allowance.

New claim 21 is further allowable or additional reasons. For example, new claim 21 recites, *inter alia*, that the write pointer register is "configurable to hold a first identifier of a storage location at which data is written into the storage buffer circuit." New claim 21 further recites, *inter alia*, that the read pointer register is "configurable to hold a second identifier, different from the first identifier, of a storage location from which data is read from the storage buffer circuit." The cited *O'Connell* reference does not have this feature. As a matter of fact, *O'Connell* teaches just the opposite. See Fig. 1; see also Col. 5, lines 27-40. The *O'Connell* reference particularly knows to begin reading when his read and write pointers have different values and knows to stop reading when his read and write pointers have a same value. Accordingly, claim 21, which requires the read pointer register to hold a value different from the value in the write pointer register, is in condition for allowance.

IV. Dependent Claims in General

Each dependent claim inherits the limitations of its respective base claim and all intervening claims. Therefore, allowance of the respective base claim compels allowance of all dependent claims. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, all

dependent claims, including those that were referenced in the Office Action and not specifically referenced in the present response, are allowable for at least reasons of their respective base claims, and the rejections should be withdrawn.

V. Conclusion

In view of the foregoing, it is respectfully submitted that independent claims 1, 15, and 21 are allowable. Dependent claims 2, and 4-14 depend from claim 1. Dependent claims 16-20 depend from claim 15. These dependent claims recite additional limitations not contained in their respective parent claims, and are therefore believed allowable as further defining over the applied references.

Overall, the *O'Connell* reference alone, or with the addition of *Fritz*, *Sadowski*, or *Cavanna* in any motivated combination, does not disclose, teach, or suggest what is recited in the independent claims. Thus, given the above remarks, it is respectfully submitted that the presently rejected independent claims are in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

If a teaching in any of the cited references that is relevant to the allowability of the claims has been overlooked, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact Mr. Satagaj at (206) 622-4900.

All of the claims remaining in the application are now clearly believed to be allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

The Director is authorized to charge any additional fees due by way of this Amendment only, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

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